

Fabrication of Sub-45-nm Structures for the Next Generation of Devices: A Lot of Effort for a Little Device

James J. Watkins and David J. Bishop,
Guest Editors

Abstract

For the last four decades, the feature sizes of electronic devices for computers have been reduced by a factor of two roughly every 18 months. The result has been a tremendous increase in computational power and reduction in the cost of computing, as measured by cost per function, of nearly 30% annually, so that computations can be done for a billionth of the cost of using the technology of the 1950s. However, devices will soon be so small that the current technology used to produce them will have reached its limits, and the graininess of individual atoms will affect their behavior. This issue focuses on techniques to make tiny devices with dimensions under 45 nm (45 billionths of a meter) for the next generation of devices. Techniques start with coupling currently used 193-nm and 157-nm optical lithography with liquid immersion to reduce the effective wavelength. Other techniques include microprinting, self-assembly, templating, and using supercritical fluids to avoid the effects of surface tension while enabling solution-based processing at such small dimensions. The development of three-dimensional structures that are approaching this scale is also discussed. The methods presented will have an effect on many areas of technology, including, in addition to electronics, advanced sensor technology, energy conversion, catalysis, and nanoelectromechanical systems.

Keywords: lithography, self-assembly, supercritical fluids, nanoelectromechanical systems.

The silicon VLSI* juggernaut is approaching an interesting transition period. For the last four decades, progress in

*VLSI stands for very-large-scale integration, referring to electronic chips with 10^5 – 10^6 transistors onboard.

miniaturizing microprocessors has been on an exponential curve, with feature sizes being reduced by a factor of two roughly every 18 months. The result has been not only a tremendous increase in computational power, but also a substantial reduction in the cost of computing, as measured

by cost per function, of nearly 30% annually.¹ Today, we fabricate transistors at literally one-billionth the cost of 1950. This kind of progress is almost without precedent in human history. The printing press did not make books a billion times cheaper. Modern agribusiness did not make food a billion times cheaper. The loom did not make clothes a billion times cheaper. But VLSI did make transistors a billion times cheaper. As a result, the world as we know it has been remarkably changed over the last 50 years. The challenge now facing us is how to stay on that exponential curve, known popularly as Moore's law, for the next 50 years. It will be quite a trick.

There are three basic challenges to maintaining Moore's law: processes and materials that allow continued reductions in size, device physics at the nanoscale, and economics. The basic working assumption of the standard CMOS (complementary metal oxide semiconductor) transistor is that matter is continuous and uniform, and devices can be continuously shrunk without having to worry about the fundamental graininess of matter, the atoms. With device features measured in micrometers, this has been a reasonable assumption for four decades. As device structures shrink to well below 100 nm, this basic working assumption will completely break down in 10–20 years. It will be impossible to build a 10-nm device that works anything like the current CMOS transistor. It will be a nanodevice with new operating principles and physics. It will also require a completely new way of making it.

That is not to say that the challenges facing VLSI fabrication based on the current CMOS design for the next 10 years will be trivial. Far from it. The international roadmap for semiconductors predicts that devices at the 45-nm node will be in production by 2010, with 32-nm devices to follow by 2013.¹ Manufacturing of these devices will require new approaches to patterning, deposition, and etching as current techniques run into fundamental roadblocks. The winning technical solution must also be an economical one: the cost of scaling to smaller dimensions cannot raise the cost of computing, storage, or memory. Moreover, any new process technology for CMOS devices will need to be seamlessly integrated into the existing Si wafer fabrication infrastructure to be broadly adapted.

In this *MRS Bulletin* theme on nanoscale device fabrication, we focus primarily on recent developments that offer great promise for the fabrication of structures below 45 nm. Much of the discussion is framed in the context of integrated circuits and data storage, but the methods dis-

cussed will have an impact on many areas of technology, including advanced sensor technology, energy conversion, catalysis, and nanoelectromechanical systems (NEMS).

As features get progressively smaller and approach molecular dimensions, the clean separation between lithography, deposition, function, and material that we were used to dealing with begins to blur. In the old days, one had a lithography tool that could pattern metals or oxides and another set of tools and techniques that could put down gold or aluminum. One could then make a transistor or an interconnect and build a DRAM (dynamic random-access memory) cell or a microprocessor. In the new nanoworld we are entering, the patterning, desired function, preparation, and material must become much more connected.

One way of achieving this is to incorporate "bottom-up" approaches such as directed self-assembly to define the smallest device features in a way that allows their marriage to traditional "top-down" techniques to functionalize the features and complete the device hierarchy. Better still is a process that yields a patterned functional material directly from a self-assembled template. Both approaches are now possible, but every function we need will require us to engineer the entire process from lithography/patterning to materials selection. It is the steps along this path that we explore in this issue.

Our general approach is to describe work that ranges from the near-term to farther out as one goes through the issue. In the first article, Rothschild and co-authors talk about UV optical lithography, the workhorse of the industry. They describe a number of novel techniques based on lens immersion that demonstrate that 193-nm and 157-nm UV light can be used

to produce high-quality 32-nm features that will find application in large-area devices, nanophotonics, nano-biology, and molecular self-assembly.

In the next article, Stewart and Willson discuss a completely new approach for nanolithography, the use of nanoimprinting, with a focus on those techniques that are assisted by ultraviolet light. In ultraviolet-assisted nanoimprint lithography (UV-NIL), a low-viscosity photosetting polymer precursor is molded using a transparent master and cross-linked by UV exposure. The technique is low-cost, rapid, and has been demonstrated for sub-5-nm horizontal pattern resolution. While the primary focus is on pattern generation for sub-45-nm integrated circuits, including imprintable dielectrics, the concept has broad application in other areas, including biomaterials and NEMS/MEMS.

Hawker and Russell then discuss the use of block copolymer self-assembly as a platform for bottom-up pattern generation. Block copolymers spontaneously organize by microphase separation into a range of well-ordered morphologies with periodicities ranging from 5 nm to 50 nm. In a crude sense, it is how biological organisms such as spiders can use local rules to produce large ordered structures such as webs. Recent advances in directed and self-orienting assembly of block copolymers now allow nearly complete control of domain alignment, orientation, and registration. The authors show how one can use these materials to create templates and structures for addressable high-density media, among other applications.

In the next article, O'Neil and Watkins talk about how we can use supercritical fluids (SCFs) to produce novel nanostructures. The properties of SCFs blur the distinction between gases and liquids, enabling solution-based processing in the

very smallest of features without concern for limitations to flow or damage from surface tension. This situation is ideal for fabrication at the nanoscale. One application is conformal metal deposition in high-aspect-ratio features. Another is the combination of SCF processing with self-assembled templates to yield precisely defined metal oxide or carbon films directly.

Finally, Yang et al. show how to use the nonlinear two-photon effect to create a novel 3D lithography. Just as multiphoton effects can be used to create new types of microscopy, they can be used to create new types of lithography that yield 3D structures directly. While the technique cannot yet be used at the 45-nm length scale, 100-nm resolution is on the way, and it will provide a means for creating topographically complex substrates for integration with the device structures produced using the methods described throughout this issue. The ability to directly write complex structures is a compelling concept, and we thought it important to include it as part of the tool kit for nanostructured devices.

One of the pleasures of being the guest editors of a special theme on nanotechnology is that one can create an entire issue on things one finds fascinating. In this issue, we have done just that. We believe that you will find the work interesting and provocative, and the results well written and engaging. We suspect that, like us, you will be in awe of what is now becoming possible. We hope that you will enjoy reading this issue as much as we enjoyed putting it together.

Reference

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James J. Watkins, Guest Editor for this issue of *MRS Bulletin*, is a professor of polymer science and engineering and co-director of MassNanoTech at the University of Massachusetts Amherst. Additionally, he is principal investigator and director of the National Science Foundation's IGERT (Integrative Graduate Education and Research Traineeship) program in nanotechnology innovation at UMass. He received his

BS and MS degrees in chemical engineering from the Johns Hopkins University and his PhD degree in polymer science and engineering from the University of Massachusetts. Between his graduate degrees, Watkins was a senior research and development engineer at Phasex Corp. in Lawrence, Mass. He joined the chemical engineering faculty at UMass in 1996 and the polymer science and engineering faculty

in 2005. His research interests include nanotechnology and materials processing in supercritical fluids.

Watkins is the recipient of the NSF Career Award, the Camille Dreyfus Teacher-Scholar Award, and a David and Lucile Packard Foundation Fellowship for Science and Engineering.

Watkins can be reached at the University of Massachusetts, Department of Polymer Science



James J. Watkins

and Engineering, Conte Polymer Research Center, 120 Governors



David J. Bishop

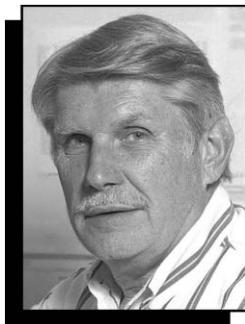
Drive, Amherst, MA 01003, USA; tel. 413-545-2569, fax 413-545-0082,



Theodore M. Bloomstein

and e-mail watkins@polysci.umass.edu.

David J. Bishop, Guest Editor for this issue of *MRS Bulletin*, is a senior researcher at Lucent Technologies. He holds a BS degree in physics from Syracuse University and MS and PhD degrees in physics from Cornell University. He joined AT&T Bell Laboratories as a postdoctoral member of staff and was made a member of the technical staff in 1979. From there, he became a Distinguished Member of the Technical Staff, the department head of Bell Laboratories, and a Bell Laboratories Fellow. He has held a number of managerial positions at Bell Labs, including director of the Liquid Crystal Physics Research Department, director of the Microstructure Physics Research Department, director of the MEMS Research Department, and vice president of Optical Research, Nanotechnology Research, Physical Sciences Research, and Enabling Physical Technologies Research. He has also served as president of Lucent Technologies' New Jersey Nanotechnology Consortium (NJNC). He has presented more than 500 papers and talks and has over



Nikolay Efremow Jr.

50 patents issued or pending.

Bishop can be reached at Lucent Technologies Inc., Room 6A-502, 600 Mountain Avenue, Murray Hill, NJ 07974, USA; tel. 908-582-3297, fax 908-582-6177, and e-mail djb@lucent.com.

Theodore M. Bloomstein is a staff member in the Submicrometer Technology Group at the MIT Lincoln Laboratory. He received an ScD degree in electrical engineering from MIT in 1996 with a doctoral thesis on laser direct-forming of three-dimensional structures in silicon. Upon joining the staff at Lincoln Laboratory, he performed the initial feasibility study of optical lithography at 157 nm, assessing optical materials, potential resist candidates, laser performance, and mask-related issues. Additionally, he has studied the effects of surface contaminants on the transmission properties of optical materials and coatings. Recently, he has been developing high-resolution patterning using optical interference techniques.

Bloomstein can be reached at the Massachusetts Institute of Technology, Lincoln Laboratory, 244 Wood Street, MS C-167, Lexington, MA 02420, USA;



Theodore H. Fedynyshyn

tel. 781-981-4671, fax 781-981-4983, and e-mail tmblooms@ll.mit.edu.

Nikolay Efremow Jr. is an assistant staff member in the Submicrometer Technology Group at the MIT Lincoln Laboratory. He received his associate degree in electrical engineering from the Franklin Institute in Boston. After finishing his military service in the Navy, he joined the Lincoln Laboratory in 1964 to test high-power microwave components used in radars. Later, he helped set up and run the photolithographic laboratory, developing the conformable lithographic mask technology. He helped to construct a cleanroom laboratory for submicrometer photolithography, where he produced state-of-the-art lithographic patterns using laser holography. He also worked on single-crystal diamond growth as well as ion-beam-assisted etching. Currently, he is developing resist processes for interference lithography.

Efremow can be reached at the Massachusetts Institute of Technology, Lincoln Laboratory, 244 Wood Street, MS I-300, Lexington, MA 02420, USA; tel. 781-981-4656, fax 781-



Michael Fritze

981-4983, and e-mail efremow@ll.mit.edu.

Theodore H. Fedynyshyn is a senior staff member in the Submicrometer Technology Group at the MIT Lincoln Laboratory. He holds a BS degree in chemistry from Lehigh University and a PhD degree in organic chemistry from Brown University. He has served in technical and program management leadership roles at Olin Corp., Shipley Co., and the Lincoln Laboratory for more than 20 years. He is a leader in the field of resists for microlithography and has published seminal papers on resist theory and performance. He has also led research efforts that developed the photoresist technology currently used by the major integrated circuit manufacturers.

Fedynyshyn can be reached at the Massachusetts Institute of Technology, Lincoln Laboratory, 244 Wood Street, MS B-181, Lexington, MA 02420, USA; tel. 781-981-7811, fax 781-981-4983, and e-mail fedynyshyn@ll.mit.edu.

Michael Fritze has been a staff member in the Advanced Silicon Technology Group at the MIT Lincoln Laboratory since 1995. He received his BS degree in physics

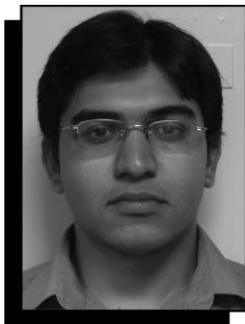


Craig J. Hawker

from Lehigh University and MS and PhD degrees in physics from Brown University. He spent several years at Bellcore between his degrees and did postdoctoral work at AT&T Bell Laboratories; both positions involved research on the electrical and optical properties of GaAs quantum-well heterostructures. His current responsibilities are in the areas of resolution-enhanced optical lithography, silicon-on-insulator device engineering, and SOI-based photonics.

Fritze can be reached at the Massachusetts Institute of Technology, Lincoln Laboratory, 244 Wood Street, MS L-212, Lexington, MA 02420, USA; tel. 781-981-2626, fax 781-981-4983, and e-mail mfritze@ll.mit.edu.

Craig J. Hawker is director of the Materials Research Laboratory at the University of California, Santa Barbara. Following his postdoctoral work with Jean Fréchet at Cornell University, he was a research staff member at the IBM Almaden Research Center from 1993 to 2004. His research focuses on the interface between organic and polymer chemistry with an emphasis on the design, synthesis, and application of well-defined



Shalin J. Jhaveri

macromolecular structures in biotechnology, microelectronics, and surface science. He has most recently been honored by the 2005 ACS Award in Applied Polymer Science and the 2005 Dutch Polymer Award, and he is listed as one of the top 100 most cited chemists worldwide over the last decade (1994–2004).

Hawker can be reached at University of California, Santa Barbara, Materials Research Laboratory, Santa Barbara, CA 93106, USA; tel. 805-893-7161, fax 805-893-4120, and e-mail hawker@mrl.ucsb.edu.

Shalin J. Jhaveri is a graduate student in the Department of Chemistry and Chemical Biology at Cornell University, working in the group of Christopher K. Ober. He received his BTech degree with a specialization in dyes and intermediates in 2002 from the University Institute of Chemical Technology in Mumbai, India. Since joining Ober's group, his research has focused on hydrogels for drug delivery and nanobiotechnology applications, two-photon lithography, and high-performance fluorescent dyes. He is a recipient of Sundar Aggarwal Award for Outstanding Indian Stu-



Christopher K. Ober

dents Entering the Department of Chemistry at Cornell University.

Jhaveri can be reached at Cornell University, Materials Science and Engineering Department, 310 Bard Hall, Ithaca, NY 14853-1501, USA; and e-mail sjj24@cornell.edu.

Christopher K. Ober is the Francis Bard Professor of Materials Engineering at Cornell University. He received his BSc degree at the University of Waterloo and his PhD degree at the University of Massachusetts in polymer science and engineering. Before accepting his current position, he worked at the Xerox Research Centre of Canada for several years. He and his research group at Cornell are currently working on problems of advanced lithography, self-assembly, and the biology–materials interface.

Ober is the recipient of the 2006 ACS Award in Applied Polymer Science, the 2004 Photopolymer Science and Technology Award, the 2003 SRC Award for Creative Invention, and the International SEMATECH Outstanding Contribution Award. He is also an associate editor of *Macromolecules* and vice president of the IUPAC Polymer Division.



Adam O'Neil

Ober can be reached at Cornell University, Materials Science and Engineering Department, 310 Bard Hall, Ithaca, NY 14853-1501, USA; tel. 607-255-8417, fax 607-255-2365, and e-mail cober@ccmr.cornell.edu.

Adam O'Neil is a post-doctoral research associate at the University of Massachusetts Amherst. He received his MSci and PhD degrees in chemistry from the University of Nottingham, England, in 1999 and 2003, respectively. He moved to UMass in 2003 and has worked for James J. Watkins in the departments of Chemical Engineering and Polymer Science and Engineering. His research interests include chemical and physical processing in supercritical solutions with applications in fullerene crystallization, mesoporous silica surface modification, and the deposition of metal and metal oxide films.

O'Neil can be reached at the University of Massachusetts, Department of Chemical Engineering, 159 Goessmann Laboratory, Amherst, MA 01003, USA; tel. 413-577-0133 and e-mail oneil@ecs.umass.edu.

Indira Pottebaum is an assistant staff member



Indira Pottebaum

in the Submicrometer Technology Group at the MIT Lincoln Laboratory. She attended Boston University, earning a BS degree in chemistry and an MS degree in physical organic chemistry. Prior to joining the Lincoln Laboratory, she worked at Telephotonics Inc. (now DuPont Photonics), where she developed, synthesized, and helped commercialize optical polymers and photoinitiators for use in integrated optical components. She has extensive experience in the synthesis, development, and characterization of novel organic materials and polymers for various optical and electronic applications, such as molecular electronics, advanced lithography, and integrated photonics.

Pottebaum can be reached at the Massachusetts Institute of Technology, Lincoln Laboratory, 244 Wood Street, MS B-187, Lexington, MA 02420, USA; tel. 781-981-4838, fax 781-981-4983, and e-mail ipottebaum@ll.mit.edu.

Mordechai Rothschild is the leader of the Submicrometer Technology Group at the MIT Lincoln Laboratory. He holds a BS degree in physics from Bar-Ilan University in Israel and a PhD degree in optics

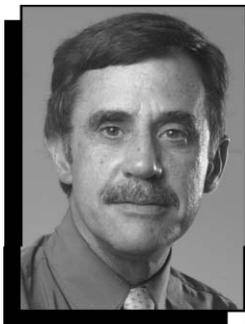


Mordechai Rothschild

from the University of Rochester. Prior to joining Lincoln Laboratory, he performed research at the University of Illinois and the University of Southern California. He currently manages several advanced lithography and nanofabrication projects, and he has played leading roles in pioneering optical lithography programs at Lincoln Laboratory, including the first 193-nm, 157-nm, and liquid-immersion lithography demonstrations and follow-on engineering projects. He has broad experience in optical systems, photochemistry, and materials processing.

Rothschild can be reached at the Massachusetts Institute of Technology, Lincoln Laboratory, 244 Wood Street, MS C-175, Lexington, MA 02420, USA; tel. 781-981-7816, fax 781-981-4983, and e-mail rothschild@ll.mit.edu.

Thomas P. Russell has been a professor of polymer science and engineering at the University of Massachusetts Amherst since 1997. He is also director of the Materials Research Science and Engineering Center on Polymers, an associate director of MassNanoTech, and director of the Multi-University Research



Thomas P. Russell

Initiative on Nanoscopic Assembly of Biologically Active Materials. He received his PhD degree in polymer science and engineering from UMass Amherst in 1979. From 1981 to 1996, he was a research staff member at the IBM Almaden Research Center in San Jose, Calif. His research interests include the surface and interfacial properties of polymers, phase transitions in polymers, directed self-assembly processes, the use of polymers as scaffolds and templates for the generation of nanoscopic structures, the interfacial assembly of nanoparticles, and the influence of supercritical fluids on phase transitions and dynamics in polymer thin films.

Russell is an associate editor of *Macromolecules* and a fellow of both the American Physical Society and the American Association for the Advancement of Science. He received the A.K. Doolittle Award in 1984, the Cooperative Research Award from the American Chemical Society in 2002, the Dutch Polymer Award in 2004, and the Polymer Physics Prize of the



Michael D. Stewart

American Physical Society in 2005. He was named a Distinguished Professor in 2004.

Russell can be reached at the University of Massachusetts Amherst, Polymer Science and Engineering Department, Conte Polymer Research Center, 120 Governors Drive, Amherst, MA 01003-9263, USA; tel. 413-577-1516, fax 413-545-0082, and e-mail russell@mail.pse.umass.edu.

Michael D. Stewart currently works for Molecular Imprints Inc., a startup company based in Austin, Texas, that develops nanoimprint tools and processes. He is also a visiting scientist/project coordinator at the University of Texas at Austin. Stewart received a bachelor's degree in chemical engineering from Vanderbilt University in 1997 and a PhD degree in chemical engineering from the University of Texas at Austin in December 2003. He is a co-author on more than 25 journal articles and conference papers in the areas of photolithography and nanoimprint lithography. His current research focus is the development of photo-



Michael Switkes

curable polymers and precursors to nanoimprint lithography applications.

Stewart can be reached at the University of Texas at Austin, Department of Chemical Engineering, M/S C0400, Austin, TX 78712-0165, USA; tel. 512-471-3906, fax 512-471-7222, and e-mail stewart@che.utexas.edu.

Michael Switkes is a staff member in the Submicrometer Technology Group at the MIT Lincoln Laboratory. He received his PhD degree in physics from Stanford University in 2000 for work on highly confined, strongly interacting electron systems and quantum dots. Since joining the Lincoln Laboratory in 1999, he has worked on projects in advanced lithography, including seminal results in liquid-immersion lithography.

Switkes can be reached at the Massachusetts Institute of Technology, Lincoln Laboratory, 244 Wood Street, MS C-135, Lexington, MA 02420, USA; tel. 781-981-4863, fax 781-981-4983, and e-mail mswitkes@ll.mit.edu.

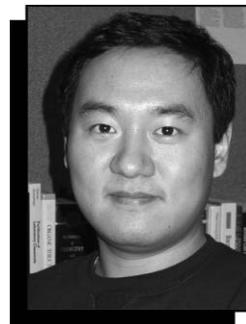


C. Grant Willson

C. Grant Willson is a professor of chemical engineering and chemistry at the University of Texas at Austin. He received his BS and PhD degrees in organic chemistry from the University of California, Berkeley, and an MS degree in organic chemistry from San Diego State University. Prior to coming to UT, he was an IBM Fellow and manager of polymer science and technology at the IBM Almaden Research Center. His research can be characterized as the design and synthesis of organic materials with an emphasis on polymers used in microelectronics applications.

Willson has received numerous awards for his research and inventions in the areas of polymer science and microelectronics. He is a member of the National Academy of Engineering and was recently named a Hero of Chemistry by the American Chemical Society. He is a co-author of more than 300 journal publications and listed as co-inventor on more than 25 issued patents.

Willson can be reached at the Univer-



Da Yang

sity of Texas at Austin, Department of Chemistry and Biochemistry, 1 University Station A5300, Austin, TX 78712-0165, USA; tel. 512-471-3975, fax 512-471-7222, and e-mail willson@che.utexas.edu.

Da Yang is an advisory engineer at the IBM Semiconductor Research and Development Center in Hopewell Junction, N.Y. He earned a BS degree in polymer chemistry from the University of Science and Technology of China and a PhD degree in organic chemistry from the University of Arizona under Seth R. Marder and David F. O'Brien. Before joining IBM in 2005, he did postdoctoral research at Cornell University, where he worked on next-generation photoresists and two-photon lithography in the laboratory of Christopher K. Ober.

Yang can be reached at IBM Logic Lithography Department, 2070 Route 52, Hopewell Junction, NY 12533, USA; tel. 845-894-3636 and e-mail dayang@us.ibm.com. □

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